DEVICE PARAMETERS 1/

JPL PART #	MFR	GENERIC PART NO.	RADIATION LEVEL (TID) (RADS) 2/	PACKAGE STYLE	TERMINAL CONNECTIONS	ELECTRICAL PERFORMANCE CHARACTERISTICS	ELECTRICAL TEST REQUIREMENTS	BURN-IN CONNECTION TABLE
12155 - E01060FR	HONEYWELL SSEC	HR1060 -BIU	100K	FIG. 5-3 HEREIN (132-LEAD FLATPACK)	FIG. 5-1 HEREIN	TABLE 4-4 & 4-5 HEREIN	TABLE 4-1 HEREIN	TABLE 4-7 HEREIN

NOTES: 1/ THIS DRAWING, IN CONJUNCTION WITH CS515837B AND MIL-I-38535, LEVEL V, IMPOSES ALL REQUIREMENTS FOR PROCUREMENT OF THESE DEVICES.
2/ THE POST-IRRADIATION PARAMETRIC LIMITS SHALL BE THOSE OF TABLES 4-4 & 4-5 HEREIN.
3/ THIS STANDARD TAKES PRECEDENCE OVER DOCUMENTS REFERENCED HEREIN.

RELEASED THRU SECTION 356 DATA MANAGEMENT: DATE:

REVISION: B APPROVED BY (Section 514): DATE:

APPROVED BY (Section 348): DATE:

APPROVED SOURCE(S)

VENDOR PART NO.	VENDOR	JPL PART NO.
22016634	HONEYWELL INC. SOLID STATE ELECTRONIC CENTER PLYMOUTH, MN 55441 CAGE NO. 34168	12155 - E01060FR

The item listed in the approved source block and identified by vendor name, address, and part number will be evaluated and tested by the JPL Electronic Parts Reliability Section or its delegated alternate before being approved for use. Non-JPL users shall check with the Electronic Parts Reliability Section on the status of the part's approval before using.

JET PROPULSION LABORATORY CALIFORNIA INSTITUTE OF TECHNOLOGY CAGE NO. 23835

Procurement Specification: CS515837

Screening Specification: CS515837, ST12155

Custodian: Parts Reliability Group Section 514

TITLE:

MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY,
BUS INTERFACE UNIT (BIU)

DETAILED SPECIFICATION

ST 12155

FILE: (Sec.514): F:\USERS\514\SPECS\ACT-DETL\ST12155.B

CHANGE INCORPORATION LOG

CHG LTR	ENGINEERING APPROVAL			PAGES AFFECTED	RELEASED THRU		
	INITIAL	SECTION	DATE		INITIAL	SECTION	DATE
A	HS LB	514 348	2/8/93 2/8/93	Initial Release	JEB	356	2/8/93
B	HS LB	514 348	4/22/94 4/22/94	2, 8, 11, 23-28, 32- 36			

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Scope

This is the detailed specification for a space-qualified Bus Interface Unit gate array ASIC for the Command and Data Subsystem. This document shall be the sole source of design specifications for the BIU gate array, and shall supersede any other specification documents issued prior to this release.

Applicable Documents

- *General Specification for Gate Array Application Specific Integrated Circuits (ASICs), 24 March 1992, CS515837, Rev. B*

  This document establishes the general design system, manufacturing and testing requirements for the gate array Application Specific Integrated Circuit (ASIC) parts.

- Preliminary *Cassini Command and Data Subsystem Bus Interface Unit Design Package, August 10, 1992, JPL D-9992*

  This document defines the functional requirements for design and performance of the Cassini Bus Interface Unit (BIU). It also provides BIU users with a functional description of the hardware and supplies the necessary timing information for a clean instrument to BIU handshake.

1. CHIP OVERVIEW

1.1 Cassini Bus Interface Unit

Communication between the CDS and other subsystems consists of commands from the CDS, status from the S/C payload subsystems, or data blocks that may pass in either direction. Data blocks may contain science data, user programs, or other information used to control or observe the status of the S/C subsystems.

All communication is initiated and controlled by the CDS 1553B Bus Controller. The BIU provides the interface between the CDS and the other Spacecraft subsystems and instruments. Because the BIU is an interface device, its fundamental functional requirements are to support the following seven interfaces; the S/C serial interface, the host generic interface, the discrete command interface, the synchronization and timing interface, the configuration/test interface, and the power ground interface. Figure 1-1 shows a block diagram of the BIU.

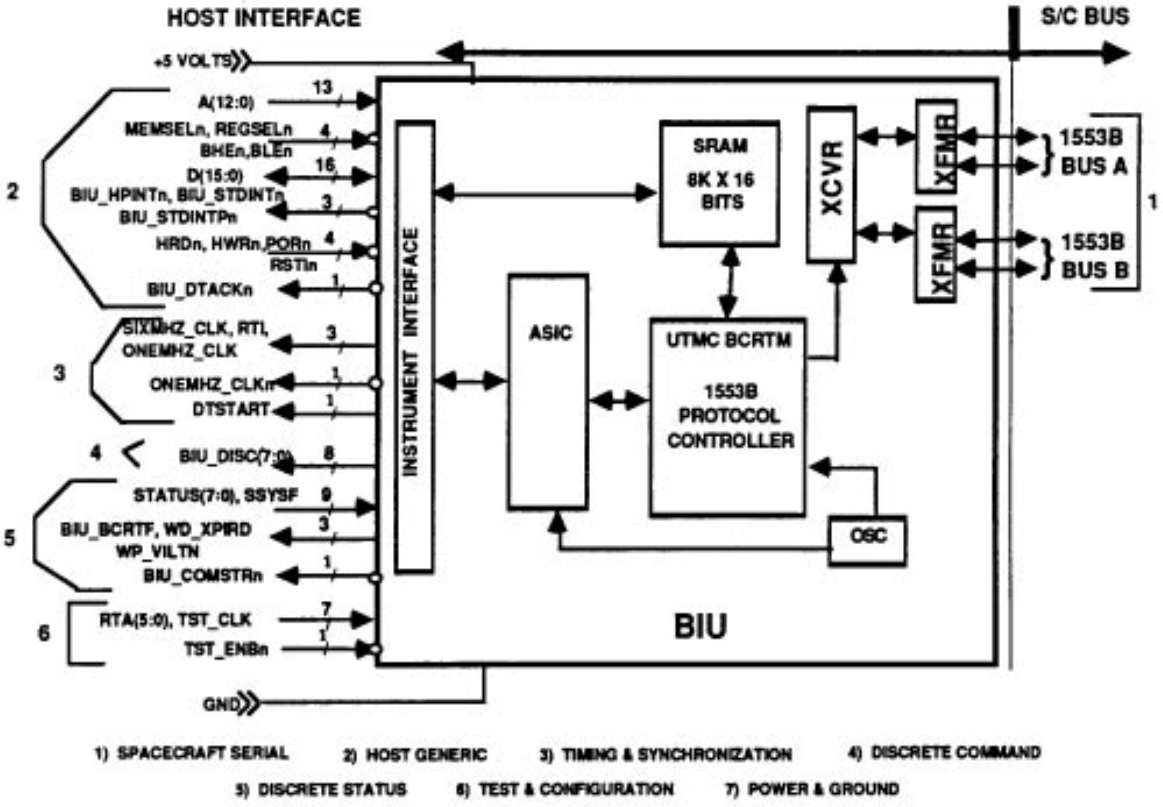


Figure 1-1. BIU ASIC in Cassini Bus Interface Unit

1.2 Bus Interface Unit (BIU) ASIC

Figure 1.2 shows a functional block diagram of the BIU ASIC. Each of these blocks will be described in the following sections.

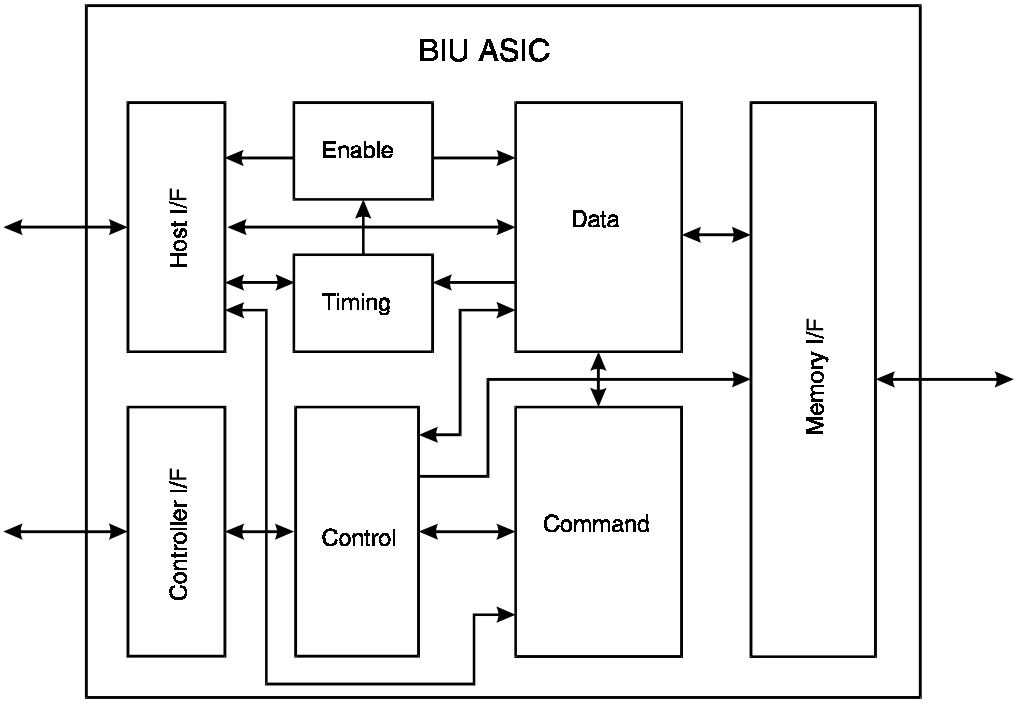


Figure 1-2. BIU ASIC Block Diagram

1.2.1 Host Interface Block

The Host interface includes the signals and protocol defined in the Cassini Bus Interface Unit Functional Requirements, JPL specification FM516008 Rev. A.

1.2.2 Controller Interface Block

The Controller interface includes the signals and protocol defined in the UTMC 1553B BCRTM Preliminary data sheet.

1.2.3 Memory Interface Block

The Memory interface includes the signals and protocol required by the SRAM memory configuration.

1.2.4 Enable Block

The Enable block provides the following capabilities:

1) Generates the controller read/write select signals as RD/WR respectively. RD/WR are sent to the control logic block where they are synchronized with the controller chip select and are output through the controller interface block as RDn and WRn.

2) Provides memory and register select arbitration. If the memory select and the register select are both active, the register select will be rendered inactive. Both the MEMSEL and REGSEL signals are sent to the control logic for Data Transfer Acknowledge (DTACKn) and memory/register select (MEM_CSIn, CSOn) generation.

3) Generates the Memory Byte High and Memory Byte Low chip enables (MBHCE, MBLCE).

4) Contains the Watchdog Timer (WDT) logic, which times the interval between each clear watchdog timer signal.

5) Generates the set watchdog timer flag signal which is sent to the Command logic where it is used to generate the watchdog timer expired signal WD_XPIRD signal.

1.2.5 Control Block

The Control block provides the following capabilities:

1) Generates the BIU_DTACKn signal which indicates that the data bus D(15:0) contains stable data ready to read into the host subsystem. BIU_DTACKn also indicates that data has been captured and written by the BIU ASIC.

2) Arbitrates host and BCRTM requests for control of the internal data bus BD(15:0). Host request is given precedence.

3) Generates the memory chip select and controller chip select signals.

4) Produces the memory write enable.

5) Produces the read/write enables for the Hardware command registers.

6) Generates the controller read/write enables which are used in conjunction with the controller chip select to enable reading from and writing to the controller chip.

7) Sets the Write Protect Violation Flag if the address bus A(12:0) addresses any memory location between 0h to 13Fh with the write protect enabled.

1.2.6 Command Block

The Command block provides the following capabilities.

1) Detects the Hardware Command Mask and Hardware Command Key data words and compares them to verify that they are complements. After verification the logic enables the command word to be written to internal registers. This logic also strips out the hardware commands, BIU_DISC(7:0), to be written to the Host I/F.

2) Generates the write protect violation flag (WP_VILTN) and the watchdog timer flag (WD_XPIRD).

3) Routes the write protect disable bit to the control logic to enable/disable the write protection on locations 0h to 13Fh.

4) Generates the clear watchdog timer signal after receipt of a data word write to memory location E000h. It also routes the watchdog timer disable bit to the enable logic to enable/disable the watchdog function.

5) Generates both the RTI and DTSTART pulse when BAI(15:0) addresses location 7984h for a data write. If the data word written is 25C3 (RTI) or A531 (DTSTART), a 500 nsec pulse is generated for each data word respectively and routed through the host interface.

1.2.7 Data block

The Data block provides the following capabilities:

1) Routes data between the memory I/F and the Host I/F.

2) Routes discrete status inputs from the Host I/F to the command block where it becomes external status data in the hardware command and status register.

3) Decodes the byte high and low enables for memory word or byte access.

4) Produces the logic reset.

5) Generates the clear watchdog timer flag and the clear write protect violation flag signals.

6) Generates the auto-initialization table which is written to the lower 320 locations of memory and to registers R2 and R0 of the BCRTM.

7) Produces the channel A or channel B inhibit which selects the active transmitter channel.

1.2.8 Timing block

The Timing block produces the following clock frequencies through divide down logic performed on a 12 MHz oscillator input.

1) 6 MHz memory clock (MCLK) frequency.

2) 1 MHz (ONEMHZ_CLK) and 1Mhz complement (ONEMHZ_CLKn) frequencies for power converter synchronization.

3) 8 Hz frequency used in the watchdog timer logic.

2. BIU ASIC SIGNAL DESIGNATIONS AND DESCRIPTIONS

Figure 2-1 shows the signal name designations of the chip, exclusive of power and ground.

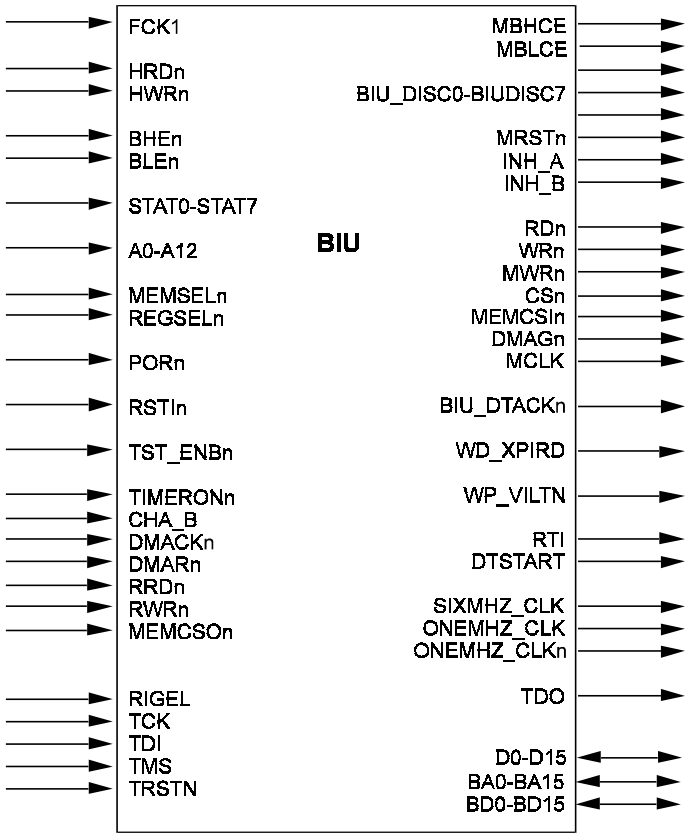


Figure 2-1. BIU ASIC Symbol

Table 2-1. Signal Descriptions

Name	Pin No.[1]	Type[2]	Drive[3]	Description
D0 - D15	70, 68, 74, 73, 78, 79, 81, 84, 69, 72 ,71, 80, 77, 82, 83, 85	BI6		Data. Bi-directional data bus to/from host.
BA0 - BA15	114, 113, 112, 110, 109, 111, 105, 103, 104, 106, 101, 102, 98, 96, 94, 97	BIRL6		BIU_ASIC address bus. Memory or control register address lines.
BD0 - BD15	121, 122, 125, 124, 129, 128, 126, 2-4, 131, 5, 6, 8, 11, 10	BIRL6		BIU_ASIC data bus. Memory or control register data.
WP_VILTN	32	OUT6	AH	Write Protect Violation. Flags write attempts to protected memory.
WD_XPIRD	37	OUT6	AH	Watchdog Expired. Flags time-out of four seconds ± 125 msec since last E000h broadcast over 1553B bus.
BIU_DTACKn	29	TRI6	ALZ	BIU Data Transfer Acknowledge. Identifies when data is on D(15:0) for reading or writing.
BIU_DISC0 - BIU_DISC7	44, 42, 47, 46, 49, 48, 50, 51	OUT6		BIU Discretes. Low byte of Hardware Command register. User defined functionality.
RTI	31	OUT6	AH	Real Time Interrupt. Driven high for 500 nsec indicating data word 25C3h has been addressed to location 7984h.
DTSTART	64	OUT6	AH	Dead Time Start. Driven high for 500 nsec indicating data word A531h has been addressed to location 7984h.
MBLCE	117	OUT6	AH	Memory Byte Low Chip Enable. Driven high to indicate memory low byte read or write.
MBHCE	119	OUT6	AH	Memory Byte High Chip Enable. Driven high to indicate memory high byte read or write.
INH_B	95	OUT6	AH	Inhibit B. Disables transmission from channel B of the BIU transceiver
INH_A	93	OUT6	AH	Inhibit A. Disables transmission from channel A of the BIU transceiver.
MRSTn	120	OUT6	AL	Master Reset. Driven low when reset conditions occur.
DMAGn	9	OUT6	AL	Direct Memory Access Grant. Driven low by a read or write enable and memory or register select.

1 The pin numbers of bus signals are in the same sequence as the signals.
2 For a description of the signal type refer to Table 4-9.
3 Drive may be active high (AH), active low (AL), active high tristate (AHZ), etc.

Table 2-1 Signal Descriptions (cont'd)

Name	Pin No.	Type	Drive	Description
ONEMHZ_CLKn	26	OUT6		One MHz Clock complement. 50% ± 5% duty cycle.
ONEMHZ_CLK	25	OUT6		One MHz Clock. 50% ± 5% duty cycle.
SIXMHZ_CLK	24	OUT6		Six MHz Clock. 50%±5% duty cycle
MEMCSIn	14	OUT6	AL	Memory Chip Select In. Drives low when memory select is active. Used in conjunction with RWRn to write to external RAM.
CSn	17	OUT6	AL	Chip Select. Drives low when register select is active.
RDn	15	OUT6	AL	Read. Drives low when host read is active.
WRn	13	OUT6	AL	Write. Drives low when host write is active.
MWRn	118	OUT6	AL	Memory Write. Drives low when addressing memory locations 0h-1FFFh.
Rigel[4]	19	INPD	AH	Rigel test command. Forces internal logic to assume functionality compatible with the Rigel test vector generation tool.
TCK[4]	21	INPD	↑	Test Circuitry Clock. When the BIUASIC is being tested using scan path logic, this is the clock for test logic.
TDI[4]	20	INPU	-	Test Data In. Serial data in for scan path test logic.
TMS[4]	23	INPU	-	Test Mode Select. Commands the BIU ASIC scan logic mode.
TRSTN[4]	22	INPU	AL	Test Reset. Forces all nodes visible to the scan paths to a known state for test purposes; not necessarily the same state values as tbd.
TDO[4]	92	TRI6	-	Test Output Data. Serial bit stream from the internal scan paths
MCLK	16	OUT6		Memory Clock. Six MHz clock frequency. 50% ± 5% duty cycle.
FCK1	18	INPD		Functional Clock. 12 MHz clock frequency. 50%±5% duty cycle.
A0 - A12	54, 56, 55, 58, 60, 62, 65, 52, 53, 57, 59, 61, 63	IN		Address bus from Host.
HRDn	91	IN	AL	Host Read. Driven low to enable data read.
TST_ENBn	28	INPU	AL	Test Enable. Enables External frequency injection.
MEMCSOn	130	IN	AL	Memory Chip Select Out. Driven low by BCRTM controller chip when memory accessed.

[4] These signals are defined for use with the Honeywell On-Chip Monitor (OCM) scan path control block, and their Rigel test vector generator. See Honeywell manuals for precise definitions of these signals. These signals are not expected to be used in flight hardware.

Table 2-1 Signal Descriptions (cont'd)

Name	Pin No.	Type	Drive	Description
BLEn	89	IN	AL	Byte Low Enable. Selects the low byte of memory for access.
BHEn	86	IN	AL	Byte High Enable. Selects the high byte of memory for access.
STAT0 - STAT7	35, 36, 39, 41, 40, 38, 43, 45	IN		Status Bits. Provide user defined status to be written into memory
RSTIn	30	IN	AL	Reset Interrupt. Initializes ASIC logic to a known state.
PORn	27	IN	AL	Power On Reset. Initializes ASIC logic to a known state. Applied at power up.
REGSELn	87	IN	AL	Register Select. Selects use of register for read or write.
MEMSELn	88	IN	AL	Memory Select. Selects use of memory for read or write.
DMACKn	12	INPU	ALZ	DMA Acknowledge. Confirms the controller receipt of DMA grant and stays active until memory access is complete.
HWRn	90	IN	AL	Host Write. Driven low to enable data write.
RRDn	127	IN	AL	RAM Read. Driven low by the controller in conjunction with MEMCSOn to read from external RAM. Monitored by the BIU_ASIC to arbitrate the use of memory.
RWRn	123	IN	AL	RAM Write. Used by the controller to enable a write to external RAM. Monitored by the BIU_ASIC arbitrate the use of memory and to detect write protection violations.
DMARn	7	INPU	ALZ	DMA Request. Controller request for RAM access.
TIMERONn	116	IN	AL	Timer On. Used in conjunction with CHA_B to provide a fail-safe 760µsec timer for transmitter channels A and B.
CHA_B	115	IN	AH	Indicates the active or last active channel. Used to produce transmitter channel inhibits (INH_A, INH_B)
VDD	34, 67, 76, 100, 107, 132	VDD	---	Vdd Power Pads.
GROUND	1, 33, 66, 75, 99, 108	VSS	---	Vss Power Pads.

3. FUNCTIONAL DESCRIPTION

The BIU ASIC is responsible for handling the functionality described below.

3.1 Auto - Initialization

The auto-initialization process involves generating a boot load kernel and writing it to the lower 320 words of BIU memory referred to as the 'auto-initialization table'. The auto-initialization table provides the capability for discrete commanding and discrete status readout, as well as the capability to receive the synchronization and timing signals, Real Time Interrupt and Dead Time Start. The auto-initialization table is always write protected from host writes. The CDS does however have the capability of disabling the write protect mechanism and over writing the 'auto-initialization table' if necessary.

The auto-initialization process is invoked after a Power On Reset (PORn), a host Reset (RSTIn) signal or after the Watchdog Timer has expired. During auto-initialization the BIU will not respond to either CDS or instrument communication.

3.2 Watchdog Function

The watchdog function verifies that communication across the 1553B bus. This verification is done via the watchdog timer which is continually reset upon receipt of a BC broadcast command to the physical address E000h. If this broadcast is not received within 4 ± .125 seconds of the last broadcast, the watchdog timer times-out and asserts the watchdog timer flag, WD_XPIRD. Auto-initialization will subsequently be invoked.

The watchdog function can be disabled over the 1553B interface using the discrete command/status registers. The status of the disable, as well as the watchdog time-out status can be read over the 1553B interface. Detailed explanation of the BIU Discrete Command/Status registers is discussed below.

3.3 BIU Discrete Command

The discrete command(hardware command) capability allows the CDS to maintain control of critical instrument resources in the event the instrument processor is not functioning correctly. Eight discrete command signals BIU_DISC(7:0) are provided for instrument use.

Additional discrete commands are issued to set and clear bits in BIU memory. These commands control the following functions: Reset watch dog timer, Disable/enable watch dog timer, Set/clear watchdog timer expiration flag, Disable/enable BIU RAM write protect, Set/clear write protect violation flag.

The CDS uses a command mask lock/key mechanism to set and change the state of the discrete commands. This mechanism, described below, reduces the probability of unintentional command acceptance.

3.3.1 Command Mask and Watchdog Timer Reset register (R/W)

BIU Physical Address: E000h

The first location is defined to be the Command Mask and Watchdog Reset register. This register, except for bit 12, is zeroed by the PORn and RSTIn signals. It is also cleared whenever data is written into the Hardware Command

register (see Section 3.3). Additionally, any write to this location will clear the Watchdog Timer. The fields within this register are described below.

Bit (11:0): Command Mask; (R/W)

The least significant 12 bits are mask bits. These bits designate which bits of the command word can be changed. Only command bits which have a 'one' set in the corresponding bit position of the mask register will be allowed to change. The command mask enables specific bits to be altered by the subsequent command word sent to E002h. This makes each command bit independently commandable. All 12 bits may be written and read.

Bit 12: External Frequency Enable; (R)

The next bit (bit 12), reflects the state of the TST_ENBn input. When this bit is high it indicates the ASIC is being driven from an external frequency source. This bit is defined as read only.

Bit (15:13): Reserved; (R)

The next 3 bits (13-15), are currently unused. These bits are always zero when read.

3.3.2 Command Key register (R/W)

BIU Physical Address: E001h

The second location is defined to be the Command Key register. The main purpose behind this register is to prevent improperly constructed commands from altering the BIU Hardware Command register. This entire register is zeroed by the PORn. Bits 0-11 are also cleared by the RSTIn signal and whenever data is written into the Hardware Command register (see Section 3.4). The fields within this register are described below.

Bit (11:0): Command Key; (R/W)

These 12 bits are used as a command key. This field must be the ones complement of the Command Mask field described above. That is, Command Mask (11:0) must equal the inverse of Command Key (11:0). Failure to meet this test will prevent the hardware command bits from being written.

Bit (15:12): Watchdog Timer Count; (R)

The next four bits (12-15) provide visibility into the current count of the Watchdog Timer. They may be read but not written. The Watchdog Timer Count is cleared whenever any write occurs to the Command Mask register (see Section 3.1).

3.3.3 Command Holding register (R/W)

BIU Physical Address: E002h

The third location is defined to be the Command Holding register. This register stores the next desired BIU command or configuration state data. The command is executed only if the mask-key test described above was successful. This entire register is zeroed by the PORn signal. The RSTIn signal will clear bits 0-11 but should not

change the state of bits 12-15. However, unlike the two previous registers, this register is not cleared by a successful write to the Hardware Command register. The fields within this register are described below.

Bit (7:0): Hardware Command Holding register; (R/W)

The least significant 8 bits (7:0) are the 'desired' hardware command bits. If the mask/key test was successful, then data placed in the Command Holding register will be moved to the Hardware Command register. The explicit assignment of hardware command bits to specific functions within the user subsystem is still TBD. In addition to mask-key mechanism, only those bits will be set or cleared in the output register which have been appropriately masked (see Section 3.1).

Bit (9:8): BIU Configuration; (R/W)

The next two bits (8 and 9) allow the CDS to establish the BIU configuration. Analogous to the Hardware Command Holding Register, these bits represent the 'desired' configuration state. BIU configuration will not change unless the mask-key test was successful. PORn and RSTIn will clear both these bits. The specifics are described below.

Bit 8: Disable BCRTM Host Write Protection. (R/W)

This bit represents the desired state of the BCRTM Write Protect mechanism. The BCRTM write protect mechanism prevents BCRTM writes to the lower 320 words (0000h to 013Fh) of BIU RAM. A one/zero written to this bit will disable/enable the BCRTM Write Protect mechanism if the appropriate mask bit is set and there is a mask-key match.

Comment: Host writes to the lower 320 words of BIU Ram are never allowed.

Bit 9: Disable BIU Watchdog Timer. (R/W)

This bit represents the desired state of the BIU Watchdog Timer Enable. A one/zero written to this bit will disable/enable the Watchdog Timer if the appropriate mask bit is set and there is a mask-key match.

Bit (11:10): BIU Error Flag management; (R/W)

The next two bits (10 and 11) allow the CDS to set and clear error flags. Analogous to the Hardware Command Holding Register, these bits represent the 'desired' BIU error flag state. PORn and RSTIn clear both these bits. The specifics are described below.

Bit 10: Load Write Protect Violation Flag. (R/W)

This bit represents the desired state of the BIU Write Protect Violation Flag (bit 13). CDS access to this bit has been provided to improve BIU and CDS testability. A one/zero written to this bit will set/clear the Write Protect Violation Flag if the appropriate mask bit is set and there is a mask-key match.

Bit 11: Load Watchdog Expiration Flag; (R/W)

This bit represents the desired state of the BIU Watchdog Expiration Violation Flag (bit 15). CDS access to this bit has been provided to improve BIU and CDS testability. Writing a one/zero to this bit sets/clears the Watchdog Expiration Flag if the appropriate mask bit is set and there is a mask-key match.

Bit (15:12): BIU Error and Status bits; (R)

These next four bits provide visibility into BIU configuration state and error status. These bits are cleared by the PORn signal but are unaffected by RSTIn.

Bit 12: Write Protect Disable Status; (R)

This bit indicates whether Write Protection is enabled or disabled. The BCRTM Write Protect mechanism prevents BCRTM writes to the lower 320 words of BIU RAM. This bit reads 'one' if Write Protection is disabled. Following a Power On Reset, BCRTM Write Protect shall be enabled (Bit 12=0). Except for the PORn signal, this bit can only be set or cleared from the CDS.

Bit 13: Write Protection Violation Flag; (R)

This bit is set whenever 'enabled' BIU Write Protection is violated. Under nominal conditions this bit should remain zero. A one indicates an attempted violation of the BIU write protection. This bit may be set or cleared from the CDS independent of whether the write protection mechanism is enabled.

Bit 14: Watchdog Disable Status; (R)

This bit indicates whether the Watchdog Timer is enabled or disabled. This bit reads 'one' if Watchdog Timer is disabled. Following a Power On Reset, the Watchdog Timer shall be enabled (Bit 14=0). Except for the PORn signal this bit can only be set or cleared from the CDS.

Bit 15: Watchdog Expired Flag; (R)

This bit is set whenever the Watchdog Timer count expires. The Watchdog Timer will expire if more than 2 seconds transpire without a write to E000h. This bit may be set or cleared from the CDS independent of whether the Watchdog Timer mechanism is enabled.

3.4 BIU Discrete Status

The BIU Discrete Status inputs, STATUS(7:0), allow the CDS to read the status of critical instrument resources without the involvement of the instrument's processor. Eight status inputs, each set and cleared by the instrument, are provided for CDS readable status.

The BIU also provides the following four discrete status outputs to the instrument: BIU BCRTM Fail (BIU_BCRTF), a static signal indicating the BCRTM has failed its self test, BIU Command Strobe (BIU_COMSTRn), a pulse indicating a valid command has been received by the BIU, Watchdog Timer Expired (WD_XPIRD), a static signal indicating the a loss of communication with the CDS, and Write Protect Violation (WP_VILTN), a static signal indicating a write attempt to the write protected auto-initialization table. The BIU Discrete Status signals are a function of the BIU Hardware Command and Status register.

3.4.1 Hardware Command and Status register

BIU Physical Address: E003h

This register is not directly write accessible from the CDS. It has the bit structure illustrated below. The fields within this register are described below.

Bit (7:0): Hardware Command Readback; (R)

The least significant 8 bits reflect the state of the hardware commands being driven into the user's subsystem from the BIU. These bits may only be altered if appropriate mask bits are set and a mask-key match has occurred. Read back of the command bits is provided to enhance the BIU's testability and to provide positive confirmation that a specific command has been executed. These bits may only be cleared by the PORn signal.

Bit (15:8): External Status; (R)

These bits provide CDS visibility into the state of specific critical user status. The assignment of bits to specific user functions is still TBD. How these bits are set or cleared is not BIU controlled.

3.5 RTI and DTSTART Distribution

The CDS distributes a Real Time Interrupt signal, RTI, at 125 millisecond intervals to ensure the software synchronization of the S/C. The CDS distributes this signal through a 1553B broadcast Mode Code (Mode Code 17, Synchronize with Data Word). The BIU translates this Mode Code into a 500 nsec wide pulse and outputs it to the instrument.

Each RTI, the CDS will broadcast the beginning of a 5 msec (minimum) dead time period on the S/C bus. Similar to RTI, CDS distributes this signal through Mode code 17, Synchronize with Data Word. The BIU ASIC translates this Mode Code into a 500 nsec wide pulse signal and outputs it to the instrument. This dead time start signal, DTSTART, guarantees the instrument a minimum of 5 msec of uninterrupted access to the BIU.

The data words associated with Mode Code 17 are mapped to location 7984h in the BIU memory space by pointers in the Remote Terminal Descriptor Table. If the data word associated with Mode Code 17 contains the bit pattern 25C3h for RTI or A531h for DTSTART, the BIU hardware will generate a 500 nsec wide pulse for each signal respectively.

3.6 Clock Sync Pulses

The BIU ASIC derives both 6 MHz and 1 MHz signals from its local 12 MHz oscillator. The 1 MHz and 1 MHz complement signals are provided to the instrument to facilitate its resident power converter synchronization. The BIU ASIC also produces a 6 MHz signal for BCRTM controller use (MCLK) and any user defined synchronization purpose. MCLK, 6 MHz, 1 MHz and 1MHz complement are inactive during power-on reset.

3.7 Host Write/Read Cycle

3.7.1 Write Cycle

To write to the BIU Memory or to a BIU register, the host processor must place the address, A(12:0), and data, D(15:0), signals on the bus, and select the appropriate memory select, MEMSELn, or register select, REGSELn, and byte high enable, BHEn, or byte low enable, BLEn, signals. The instrument initiates the write cycle by driving the write signal, HWRn, low. When the BIU ASIC has completed the write it will activate BIU_DTACKn. The host then terminates the cycle by deasserting the write signal HWRn. BIU_DTACKn will become inactive after the HWRn is deactivated.

The host write cycle is an asynchronous handshake. Metastability issues pertaining to the critical control signals are handled by the BIU design as follows; if REGSELn and MEMSELn should overlap, then MEMSELn will take precedence, if HRDn and HWRn should overlap, then HWRn will take precedence.

3.7.2 Read Cycle

The BIU ASIC read cycle is similar to that of a write cycle. The host must place the address, A(12:0), and select the appropriate memory select, MEMSELn, or register select, REGSELn, and byte high enable, BHEn, or byte low enable, BLEn, signals. The instrument initiates the read by driving the read signal, HRDn, low. When the BIU has placed the requested data on the bus, D(15:0), it will activate BIU_DTACKn. The host can then latch the data and terminate the read cycle by deasserting the HRDn. BIU_DTACKn will become inactive after HRDn is deactivated. Metastability issues pertaining to the critical control signals are handled by the BIU as stated above in the Write Cycle description.

4. ELECTRICAL CHARACTERISTICS

4.1 Electrical Test Requirements

Test	Subgroups (Per MIL-STD-883, Method 5005, Table 1)
Initial (Pre Burn-In)	1,7
Interim (Post Static I Burn-In)	1*,7*
Delta Calculations*,**	
Interim (Post Static II Burn-In)	1*,7*
Delta Calculations*,**	
Final (Post Dynamic Burn-In)	1*,2,3,7*,8,9,10,11
Delta Calculations*,**	
Group A	1,2,3,7,8,9,10,11
Group C End Point electrical***	1,2,3,7,8,9,10,11
Delta Calculations**	

Table 4-1. Electrical Test Requirements

* PDA applies to these subgroups

** Deltas shall be calculated relative to the initial electrical parameters. Delta limits of Table 4-8 herein shall apply.

*** Group C Lifetest shall be performed using the dynamic burn-in configuration of Table 4-7 herein.

4.2 Absolute Maximum Ratings[5,6,7]

Symbol	Parameter	Ratings		Units
		Min.	Max.	
V_{DD}	Supply Voltage	-0.5	7.0	V
V_{IN}	Input Voltage Range	GND - 0.5	V_{DD} + 0.5	V
I_{OUT}	DC or max. Output Current		50	mA
P_D	Max. Package Power Dissipation		4	W
T_{ST}	Storage Temperature Range	-65	150	^oC
T_S	Lead Temperature (Soldering, 5s)		270	^oC
T_J	Junction Temperature		175	^oC
Θ_{JC}	Thermal Resistance, Junction to Case		4	$^oC/W$
V_{ESD}	ESD Protection Voltage - Class 2 (MIL-STD-883, Method 3015)	2000		V

Table 4-2. Absolute Maximum Ratings

4.3 Recommended Operating Conditions [7,8]

Symbol	Parameter	Ratings		Units
		Min.	Max.	
V_{DD}	Supply Voltage	4.5	5.5	V
T_A	Ambient Temperature	-55	125	^oC
f_{max}	Max. Operating Frequency		12	MHz
t_r, t_f	Input Rise Time, Input Fall Time		500	ns

Table 4-3. Recommended Operating Conditions.

5 Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and effect reliability.
6 Values are guaranteed but not tested.
7 $-55^oC \le T_c \le 125^oC$ except as noted.
8 Extented operation outside recommended limits may degrade performance and effect reliability.

4.4 DC Characteristics

4.4.1 DC Electrical Performance Characteristics

Parameter	Symbol	Test Condition	Subgroup	Limit		Unit
				Min	Max	
Input Threshold Voltage	V_{IH1} [9]	V_{DD}=5.5V	1,2,3		3.85	V
	V_{IH2} [10]	V_{DD}=5.5V	1,2,3		4.50	V
	V_{IL}	V_{DD}=4.5V	1,2,3	1.35		V
Input Leakage Current	I_{IH1} [11]	V_{DD}=5.5V, V_{IH}=V_{DD}	1,2,3	-10	10	µA
	I_{IH2} [12]	V_{DD}=5.5V, V_{IH}=V_{DD}	1,2,3	-10	10	µA
	I_{IH3} [13]	V_{DD}=5.5V, V_{IH}=V_{DD}	1,2,3	50	550	µA
	I_{IL1} [11]	V_{DD}=5.5V, V_{IL}=GND	1,2,3	-10	10	µA
	I_{IL2} [12]	V_{DD}=5.5V, V_{IL}=GND	1,2,3	-550	-50	µA
	I_{IL3} [13]	V_{DD}=5.5V, V_{IL}=GND	1,2,3	-10	10	µA
Output Leakage Current	I_{OZH} [14]	V_{DD}=5.5V, V_O=VDD	1,2,3	-10	10	µA
(Tristate)	I_{OZL} [14]	V_{DD}=5.5V, V_O=GND	1,2,3	-10	10	µA
Ringlatch Current Low	I_{OL_RL1} [15]	V_{DD}=4.5V, V_{OL}=0.5V	1,2,3	60	280	µA
	I_{OL_RL2} [15]	V_{DD}=4.5V, V_{OL}=1.0V	1,2,3	110	510	µA
	I_{OL_RL3} [15]	V_{DD}=5.5V, V_{OL}=2.0V	1,2,3	150	1040	µA
Ringlatch Current High	I_{OH_RL1} [15]	V_{DD}=4.5V, V_{OH}=4.0V	1,2,3	-85	-10	µA
	I_{OH_RL2} [15]	V_{DD}=4.5V, V_{OH}=3.5V	1,2,3	-150	-20	µA
	I_{OH_RL3} [15]	V_{DD}=5.5V, V_{OH}=3.5V	1,2,3	-290	-20	µA
Output Current	I_{OH}	V_{DD}=4.5V, V_{OH}=4.0V	1,2,3		-6	mA
	I_{OL}	V_{DD}=4.5V, V_{OL}=0.5V	1,2,3	6		mA
Output Voltage	V_{OH}	V_{DD}=4.5V, I_{OH}=-6mA	1,2,3	4.0		V
	V_{OL}	V_{DD}=4.5V, I_{OL}=6mA	1,2,3		0.5	V

Table 4-4. DC Performance Characteristics

---

9 All inputs, except TRSTN.
10 TRSTN
11 All inputs, except inputs with Pull-Ups and Pull-Downs.
12 Inputs with Pull-Ups: TDI, TMS, TRSTN, DMACKn, DMARn, TST_ENBn
13 Inputs with Pull-Downs: TCK, Rigel, FCK1
14 Bidirectionals and Tristates: BIU_DTACKn, D0 - D15, TDO
15 Bidirectionals with Ringlatch: BA0 - BA15, BD0 - BD15

Parameter	Symbol	Test Condition	Subgroup	Limit		Unit
				Min	Max	
Standby Supply Current	I_{DDSB}	V_{DD}=5.5V, V_{IN}=V_{DD} or GND, Fc=0 Hz	1,2,3		800	uA
Quiescent Current	I_{DDQ}	V_{DD}=5.5V, V_{IN}=V_{DD} or GND, Fc=0 Hz	1		5	uA
Operating Current	I_{DDOP}	V_{DD}=5.5V, V_{IN}=V_{DD} or GND, Fc=12MHz	1,2,3		50	mA
Input Capacitance [16]	C_{IN}				15	pF
Output Capacitance [16,17]	C_{OUT}				15	pF

Table 4-4. DC Performance Characteristics (Cont'd)

4.4.2 Estimated Power Dissipation.

$P_{Total} = P_{Internal} + P_{Outputs} + P_{Quiescent} = 170 + 25 + 4.4 = 199.4$ mW

$P_{Internal} = {}^{1}/_{2} * f_{CLK} * C_{Lint} * (V_{DD})^2 = 170$ mW

Where:
- C_{Lint} = S * #of Nets * 0.75pf
- S = 0.25
- #of Nets = 5000
- f_{CLK} = 12 MHz
- V_{DD} = 5.5V

$P_{Outputs} = {}^{1}/_{2} * f_{CLK} * C_{Lout} * (V_{DD})^2 + P_{Crowbar} = 22.7 + 2.3 = 25$ mW

Where:
- C_{Lout} = S * #of Output Pads * 50 (25) pf
- S = 0.04
- #of Output Pads = 48 @ 50 pF; 29 @ 25 pF
- f_{CLK} = 12 MHz
- V_{DD} = 5.5V
- $P_{Crowbar}$ = 10% of $P_{Outputs}$

[16] Guaranteed but not tested.
[17] Refers to internal capacitance.

$P_{Quiescent} = V_{DD} * I_{DDSB} = 4.4\ mW$

Where: $V_{DD} = 5.5V$
$I_{DDSB} = 800\ \mu A$

4.4.3 IDDQ Testing.

Quiescent Current (IDDQ) testing shall be accomplished by using the Stuck-at Fault test vectors generated with RIGEL, or a subset thereof, as determined by JPL. Measurements shall be taken at every vector, unless otherwise indicated, recorded and compared to the IDDQ limit. The following statistical values shall be provided: Minimum, Maximum, Mean, Standard Deviation. The IDDQ limits shall be established by JPL after characterization of Engineering Model parts which are fabricated from the same wafer lot as the flight parts.

4.4.4 Pulldown Resistors.

The internal pulldown resistor design option has been used on the following input pads:

TCK
Rigel
FCK1

It is recommended that the TCK and Rigel signals be tied low (logic 0) in the flight hardware.

4.4.5 Pullup Resistors.

The internal pullup resistor design option has been used on the following input pads:

TDI
TMS
TRSTN
DMACKn
DMARn
TST_ENBn

It is recommended that the TDI and TMS signals be tied high (logic 1) in the flight hardware. TRSTN must be held low during power-up and therefore is recommended to be tied low (logic 0).

4.4.6 Ring Latches.

Certain signals are required to be held at a valid logic state in flight. The internal ring latch design option shall be used on the following pads to assure a valid logic state:

4.4.6.1 Bidirectionals with Ring Latches.

BA0 - BA15
BD0 - BD 15

4.5 AC Characteristics

4.5.1 AC Electrical Performance Characteristics

Parameter	Symbol	Test Condition $V_{IN}=V_{DD}$ or GND	Subgroup	Specification Limit		Tester Limit[18,19]		Unit
				Min	Max	Min	Max	
Functional Tests		V_{DD}=4.5 & 5.5V Fc=12 MHz	7,8	pass		pass		
Propagation Delay:		V_{DD}=4.5 & 5.5V Fc=500 kHz	9,10,11					
FCK1 to MCLK	t_{PLH1} t_{PHL1}		9,10,11		33.8 33.8		32.2 31.8	ns ns
FCK2 to PROP1[20]	t_{PLH2} t_{PHL2}		9,10,11	3.9 3.7	75.1 50.1	3.9 3.7	73.5 48.1	ns ns
FCK2 to PROP2[21]	t_{PLH3} t_{PHL3}		9,10,11	3.9 3.7	88.2 50.1	3.9 3.7	86.6 48.1	ns ns
Set-up Time:		V_{DD}=4.5 & 5.5V Fc=500 kHz	9,10,11					
RWRn to FCK1	t_{SU}				13.5		13.5	ns
Hold Time:		V_{DD}=4.5 & 5.5V Fc=500 kHz	9,10,11					

Table 4-5. AC Performance Characteristics

4.5.2 Timing Analysis.

Pre-layout and post-layout timing shall pass the QuickSim simulation of the vectors supplied to the contractor without setup/hold timing violations.

BIU ASIC **"Set-up times"**, **"Hold times"**, and **"Propagation Delays"** can be **+ / -** 20% of pre-routing values with the exception of the two nets associated with the critical path which should be made as short as practical to be less sensitive to interfacing chip parameters!

Two nets to be as short as practical are:

1. **RWRn (input pad I$10222) to /M/I$1069** (a shift register)
2. **6MHZ (/T/I$8) to MCLK** (output pad I$3903)

Note: Each net has a single path between elements.

---

18 Tester limits are shown from a test perspective (i.e., set-up time, hold time are shown as max. limits).

19 Tester limits do not include guardbanding for tester errors.

20 Pingroup PROP1 consists of D0 - D15, BIU_DISC0 - BIU_DISC7, DMAGn, WRn, MEMCSIn, RDn, MCLK, CSn, SIXMHZ_CLK, ONEMHZ_CLK, ONEMHZ_CLKn, DTSTART, RTI, WP_VILTn, WD_XPIRD, MRSTn.

21 Pingroup PROP2 consists of MBLCE and MBHCE.

4.5.2.1 Pre-Layout Timing Margins.

Pre-layout timing margins shall be calculated by using standard extreme-value analysis. The extreme values for the cell library shall be supplied by the contractor. Critical paths will be identified and margin calculated via Mentor or Honeywell software toolsets, or a combination thereof.

4.5.2.2 Post-Layout Timing Margins.

Post-layout analysis of the device shall show positive margin on internal critical paths over all operating conditions. The analysis will follow the same form as the pre-layout analysis, with the post-layout timing values annotated to the design file by the contractor.

4.5.2.3 Tester Specification Limits.

Tester Specification limits in Table 4-5 have been adjusted for modified output levels and for differences in output loading in the ANDO tester environment. Modified output levels are required to account for impedance mismatches between device outputs and the ANDO tester environment. The level at which an output is considered to have switched has been changed from 50% of VDD to 1V for low to high transitions and VDD-0.5V for high to low transitions for the 3mA buffer and to 1V for low to high transitions and VDD-1V for high to low transitions for the higher drive buffers (6mA, 9mA, 12mA, 15mA).

$t_{SPEC}(\text{Tester}) = t_{SPEC}(\text{System}) - (T_{Offset\_fixed} + \text{CLoad} * \text{LoadingFactor})$

Where:

C_{Load} = 25 pF (System Load, Outputs)
C_{Load} = 50 pF (System Load, Bidirectionals)

For 6 mA drive buffer:

Low to High transition:	T_{Offset_fixed} = -1.0 ns	LoadingFactor = 0.103
High to Low transition:	T_{Offset_fixed} = -1.0 ns	LoadingFactor = 0.121

4.5.3 Tester Load Circuit

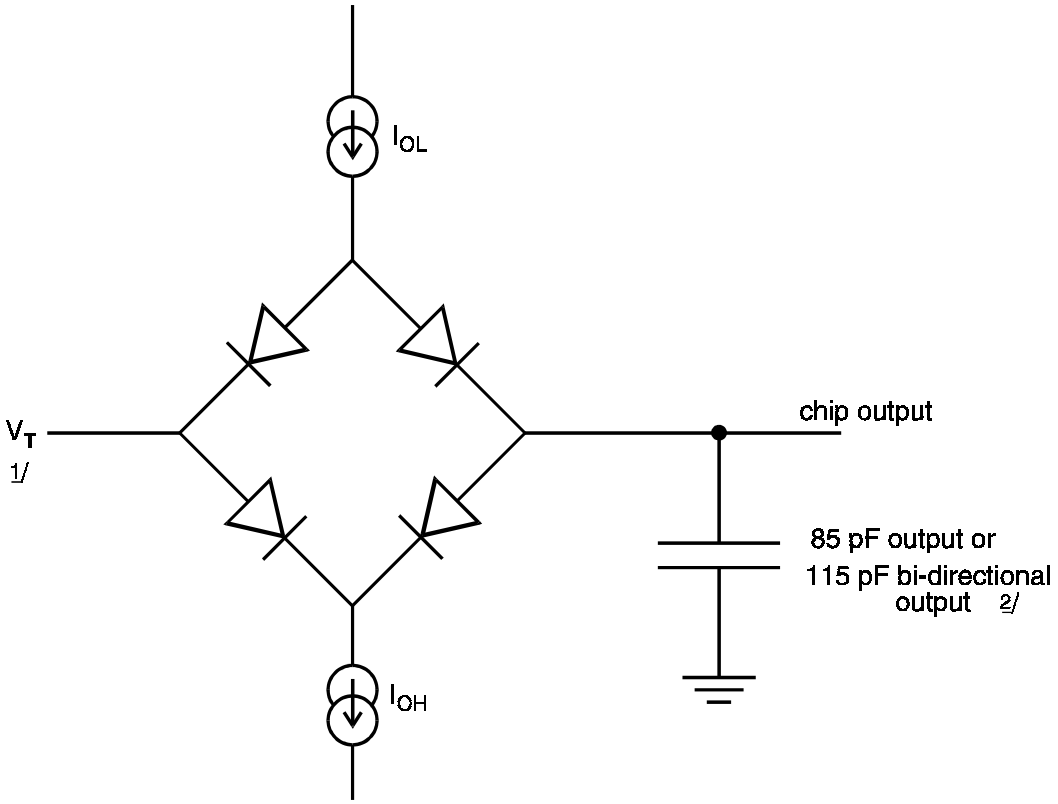


Figure 4-3. Tester Load Circuit

1/ V_T is a variable dependent upon the test parameter.
2/ This capacitance is actually partially distributed through the fixturing so that the device is actually loaded by a transmission line.

4.6 Burn-In

4.6.1 Static Burn-In

The Static Burn-In conditions shall be as specified in JPL General Specification CS 515837, Rev. B. The burn-in configuration shall be as shown in Table 4-7.

4.6.2 Dynamic Burn-In

The Dynamic Burn-In conditions shall be as specified in JPL General Specification CS 515837, Rev. B. The burn-in configuration shall be as shown in Table 4-7. Input stimuli (STIM) to exercise the device shall be applied by using the RIGEL Stuck-at Fault test vectors, or a subset thereof, as determined by JPL. At least one output (MON) shall be monitored during burn-in to assure that the output is toggled and the circuit functioning.

4.6.3 Burn-In Conditions

	Static I	**Static II**	**Dynamic**	**QCI - Life Test**
Duration	48 hours	48 hours	240 hours	2000 hours
Voltage	6.5 V	6.5 V	6.5 V	6.0 V
+ Tolerance	+0.1V	+0.1V	+0.1V *	+0.1V *
- Tolerance	-0.25V	-0.25V	-0.25V	-0.25V
Temperature	125 ^{O}C	125 ^{O}C	125 ^{O}C	125 ^{O}C
+ Tolerance	+5 ^{O}C	+5 ^{O}C	+5 ^{O}C	+5 ^{O}C
- Tolerance	-0 ^{O}C	-0 ^{O}C	-0 ^{O}C	-0 ^{O}C

Table 4-6. Burn-In Conditions

* Applies to Average Power Supply Voltage. Tolerance for Dynamic Switching Noise is +0.25V.

4.6.4 Burn-In Configuration

Pin Name	Pin No.[22]	Type[23]	Burn-In Test Connection[24]			Description
			Static I	Static II	Dynamic	
D0 - D15	70, 68, 74, 73, 78, 79, 81, 84, 69, 72 ,71, 80, 77, 82, 83, 85	BI6	GND	VDD	VDD	Data.
BA0 - BA15	114, 113, 112, 110, 109, 111, 105, 103, 104, 106, 101, 102, 98, 96, 94, 97	BIRL6	GND	VDD	VDD	BIU_ASIC address bus.
BD0 - BD15	121, 122, 125, 124, 129, 128, 126, 2-4, 131, 5, 6, 8, 11, 10	BIRL6	GND	VDD	VDD	BIU_ASIC data bus.
WP_VILTN	32	OUT6	GND	VDD	VDD	Write Protect Violation.
WD_XPIRD	37	OUT6	GND	VDD	VDD	Watchdog Expired.
BIU_DTACKn	29	TRI6	GND	VDD	VDD	BIU Data Transfer Acknowledge.
BIU_DISC0 - BIU_DISC7	44, 42, 47, 46, 49, 48, 50, 51	OUT6	GND	VDD	VDD	BIU Discretes.
RTI	31	OUT6	GND	VDD	VDD	Real Time Interrupt.
DTSTART	64	OUT6	GND	VDD	VDD	Dead Time Start.
MBLCE	117	OUT6	GND	VDD	VDD	Memory Byte Low Chip Enable.
MBHCE	119	OUT6	GND	VDD	VDD	Memory Byte High Chip Enable.
INH_B	95	OUT6	GND	VDD	VDD	Inhibit B.
INH_A	93	OUT6	GND	VDD	VDD	Inhibit A.
MRSTn	120	OUT6	GND	VDD	VDD	Master Reset.
DMAGn	9	OUT6	GND	VDD	VDD	Direct Memory Access Grant.
ONEMHZ_CLKn	26	OUT6	GND	VDD	VDD	One MHz Clock complement.
ONEMHZ_CLK	25	OUT6	GND	VDD	VDD	One MHz Clock.
SIXMHZ_CLK	24	OUT6	GND	VDD	VDD	Six MHz Clock.
MEMCSIn	14	OUT6	GND	VDD	VDD	Memory Chip Select In.
CSn	17	OUT6	GND	VDD	VDD	Chip Select.
RDn	15	OUT6	GND	VDD	VDD	Read.
WRn	13	OUT6	GND	VDD	VDD	Write.
MWRn	118	OUT6	GND	VDD	VDD	Memory Write.

Table 4-7. Burn-In Configuration

[22] The pin numbers of bus signals are in the same sequence as the signals.
[23] For a description of the signal type refer to Table 4-9.
[24] All inputs and outputs shall be tied to the specified voltage level through a 2.2 kΩ resistor (±5%, 1/4W).

Pin Name	Pin No.[25]	Type[26]	Burn-In Test Connection[27]			Description
			Static I	Static II	Dynamic	
Rigel	19	INPD	GND	VDD	STIM[28]	Rigel test command.
TCK	21	INPD	GND	VDD	STIM[21]	Test Circuitry Clock.
TDI	20	INPU	GND	VDD	STIM[21]	Test Data In.
TMS	23	INPU	GND	VDD	STIM[21]	Test Mode Select
TRSTN	22	INPU	GND	VDD	STIM[21]	Test Reset
TDO	92	TRI6	GND	VDD	MON[29]	Test Output Data
MCLK	16	OUT6	GND	VDD	VDD	Memory Clock.
FCK1	18	INPD	GND	VDD	VDD	Functional Clock.
A0 - A12	54, 56, 55, 58, 60, 62, 65, 52, 53, 57, 59, 61, 63	IN	GND	VDD	VDD	Address bus from Host.
HRDn	91	IN	GND	VDD	VDD	Host Read.
TST_ENBn	28	INPU	GND	VDD	VDD	Test Enable.
MEMCSOn	130	IN	GND	VDD	VDD	Memory Chip Select Out.
BLEn	89	IN	GND	VDD	VDD	Byte Low Enable.
BHEn	86	IN	GND	VDD	VDD	Byte High Enable.
STAT0 - STAT7	35, 36, 39, 41, 40, 38, 43, 45	IN	GND	VDD	VDD	Status Bits.
RSTIn	30	IN	GND	VDD	VDD	Reset Interrupt.
PORn	27	IN	GND	VDD	VDD	Power On Reset.
REGSELn	87	IN	GND	VDD	VDD	Register Select.
MEMSELn	88	IN	GND	VDD	VDD	Memory Select.
DMACKn	12	INPU	GND	VDD	VDD	DMA Acknowledge.
HWRn	90	IN	GND	VDD	VDD	Host Write.
RRDn	127	IN	GND	VDD	VDD	RAM Read.
RWRn	123	IN	GND	VDD	VDD	RAM Write.
DMARn	7	INPU	GND	VDD	VDD	DMA Request.
TIMERONn	116	IN	GND	VDD	VDD	Timer On.
CHA_B	115	IN	GND	VDD	VDD	Ative or last active channel.
VDD	34, 67, 76, 100, 107, 132	VDD	6.5V	6.5V	6.5V (6V for Lifetest)	Vdd Power Pads.
GROUND	1, 33, 66, 75, 99, 108	VSS	0.0V	0.0V	0.0V	Vss Power Pads.

Table 4-7. Burn-In Configuration (Cont'd)

[25] The pin numbers of bus signals are in the same sequence as the signals.
[26] For a description of the signal type refer to Table 4-9.
[27] All inputs and outputs shall be tied to the specified voltage level through a 2.2 kΩ resistor (±5%, 1/4W).
[28] Stimulated Inputs
[29] Monitored Output

4.6.5 Delta Limits

Symbol	Parameter	Spec. Limits		Units	Delta Limits	Units
		Min	Max			
I_{DDSB}	Static Supply Current		800	µA	80	µA
I_{IL1}	Input Leakage Current Low	-10	10	µA	±1	µA
I_{IL2}	Input Leakage Current Low, Pull-Ups	-550	-50	µA	±55	µA
I_{IL3}	Input Leakage Current Low, Pull-Downs	-10	10	µA	±1	µA
I_{IH1}	Input Leakage Current High	-10	10	µA	±1	µA
I_{IH2}	Input Leakage Current High, Pull-Ups	-10	10	µA	±1	µA
I_{IH3}	Input Leakage Current High, Pull-Downs	50	550	µA	±55	µA
I_{OZL}	Output Leakage Current Low	-10	10	µA	±1	µA
I_{OZH}	Output Leakage Current High	-10	10	µA	±1	µA
I_{OL_RL1}	Ringlatch Current Low	60	280	µA	±22	µA
I_{OL_RL2}		110	510	µA	±40	µA
I_{OL_RL3}		150	1040	µA	±89	µA
I_{OH_RL1}	Ringlatch Current High	-85	-10	µA	±8	µA
I_{OH_RL2}		-150	-20	µA	±13	µA
I_{OH_RL3}		-290	-20	µA	±27	µA
I_{OL}	Output Current Low		-6	mA	±600	µA
I_{OH}	Output Current High	6		mA	±600	µA

Table 4-8. Delta Limits

4.7 Pin Type Description

Pin Name		Drive	I/O	Type
BI6	=	6mA,	CMOS,	Bidirectional Signal
BIRL6	=	6mA,	CMOS,	Bidirectional Signal with Ring Latch
IN	=		CMOS,	Input Signal
INPU	=		CMOS,	Input Signal with Pull-up
INPD	=		CMOS,	Input Signal with Pull-down
TRI6	=	6mA,	CMOS,	Tri-State Signal
OUT6	=	6mA,	CMOS,	Output Signal

Table 4-9. Pin Type Description

5. PHYSICAL CHARACTERISTICS

5.1 Pin Assignment.

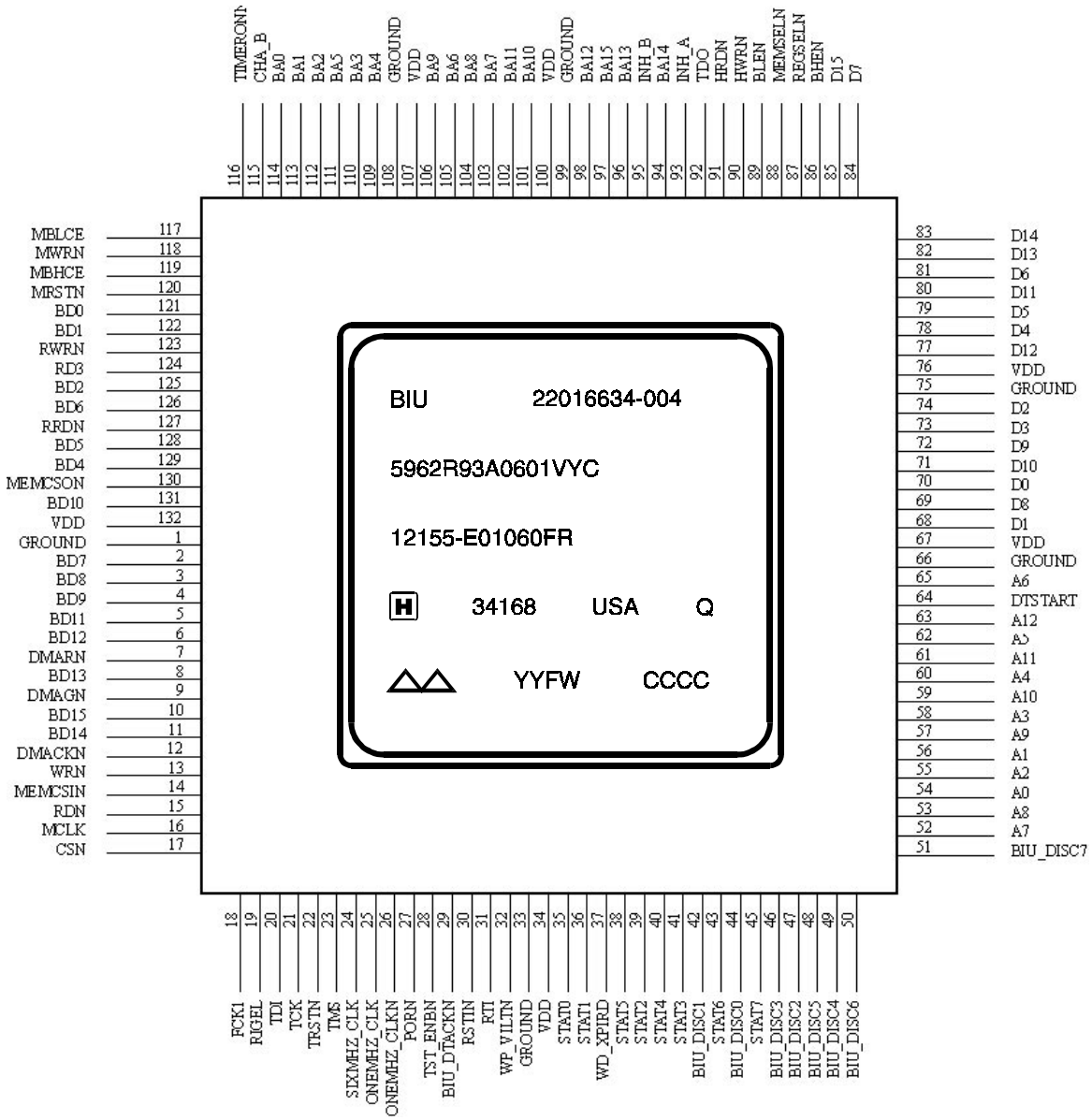
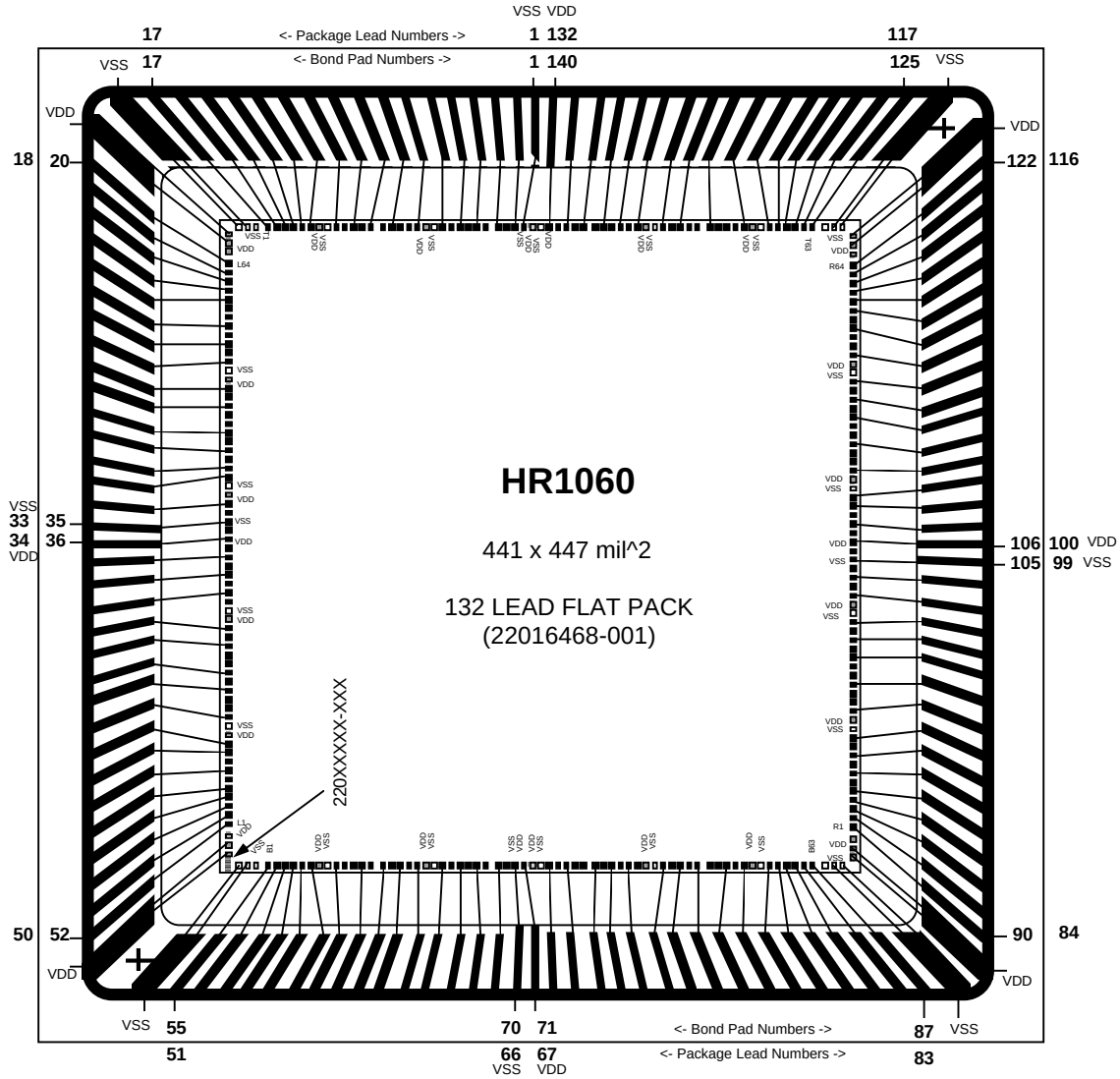


Figure 5-1. BIU ASIC Pinout Assignments

5.2 Bonding Diagram [30]



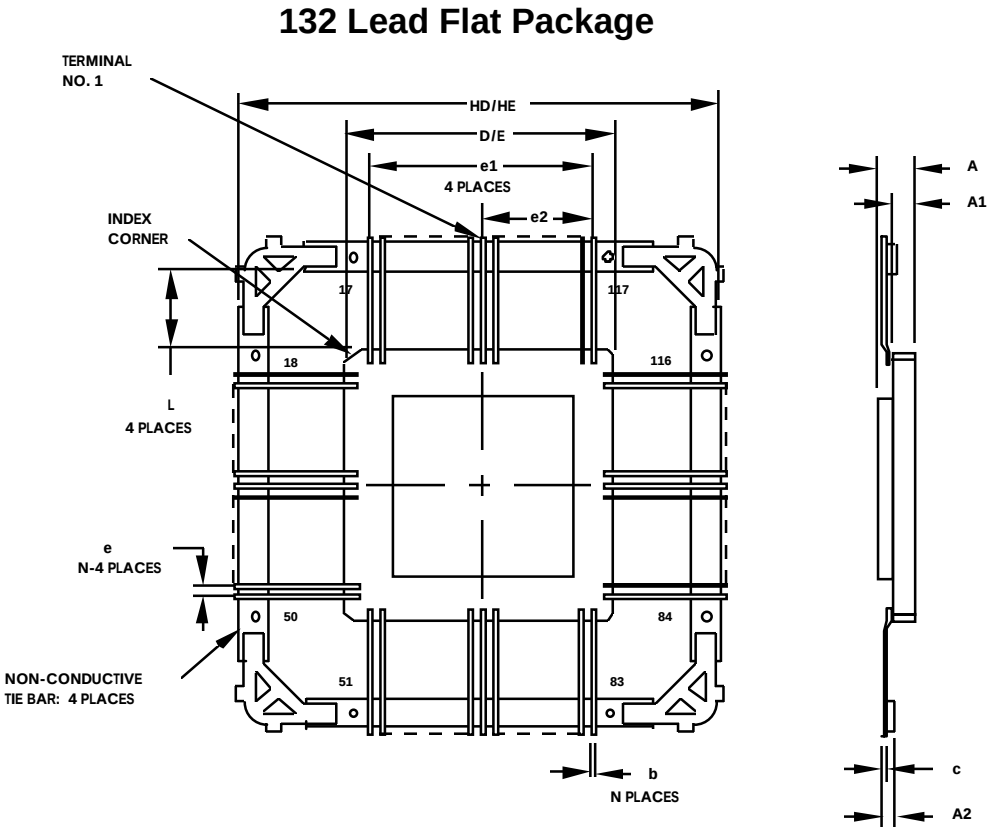
Die Cavity: 520 mil/side
VDD Plane: pins 34, 67, 100, 132
VSS Plane: pins 1, 33, 66, 99
Die Attach: VSS
Lid and Seal Ring: VSS

Figure 5-2. Bonding Diagram (132 pin Flatpack)

30 Designer assigned extra VSS and VDD pads and pins:

VSS - Pin # 75, Pad Loc. # B50; Pin # 108, Pad Loc. # R51
VDD - Pin # 76, Pad Loc. # B53; Pin # 107, Pad Loc. # R49

5.3 Package Outline.



PACKAGE DIMENSIONS			
Symbol	Dimensions in inches		
	min		max
A	0.085		0.115
A1	-		0.095
A2	0.035		0.050
b	0.007		0.011
c	0.005		0.008
D/E	0.940		0.960
e		0.025 BSC	
e1		0.800 BSC	
e2		0.400 BSC	
HD/HE	2.485		2.515
L	0.550		-
N	132		

Figure 5-3. Package Outline (132 pin Flatpack)

5.4 Marking Diagram

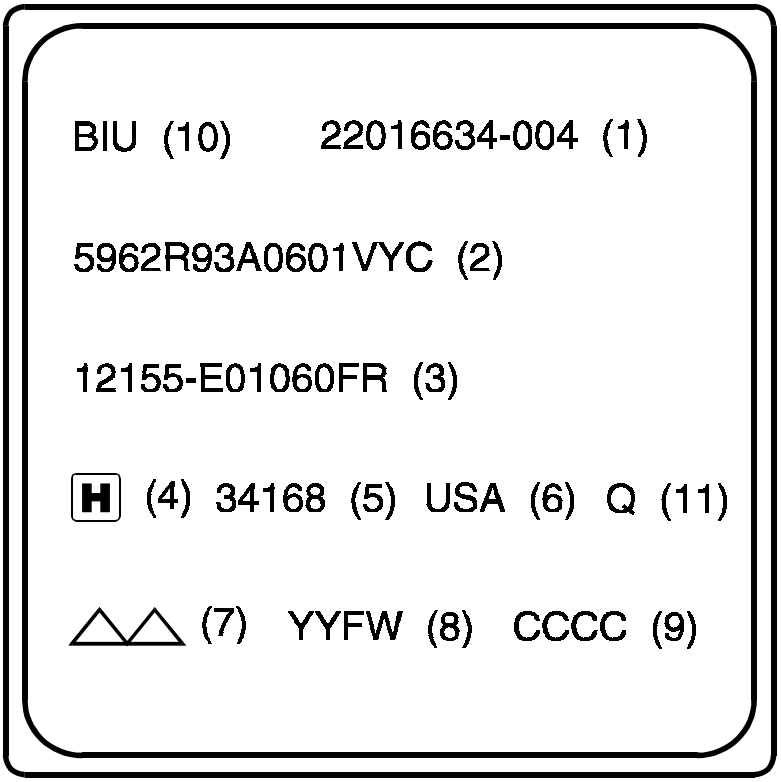


Figure 5-4. Marking Diagram

(1) Honeywell Part Number
(2) QML Number (Flight Units only)
(3) Customer Part Number
(4) Honeywell Trademark
(5) Federal Supplier Manufacturing Number
(6) Country of Origin
(7) Pin 1 indicator and ESD identifier
(8) Date Code -Year and Fiscal Week of Lid Seal.
YY = Year
FW = Fiscal Week
(9) Serialization (Traceability Capability to Die)
(10) Chip Name (If required)
(11) QML Mark (Flight Units only)

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